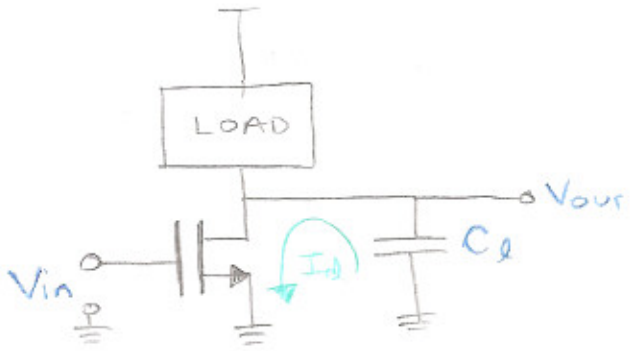
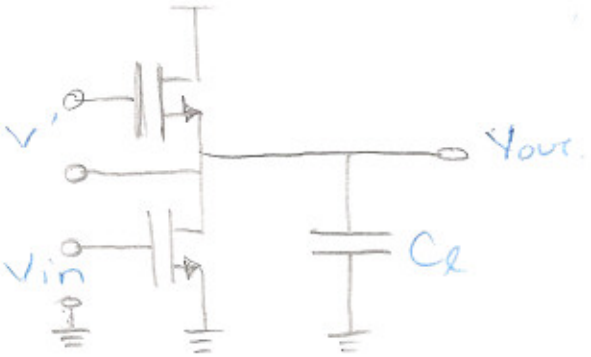
n-MOS LOGIC CIRCUITS

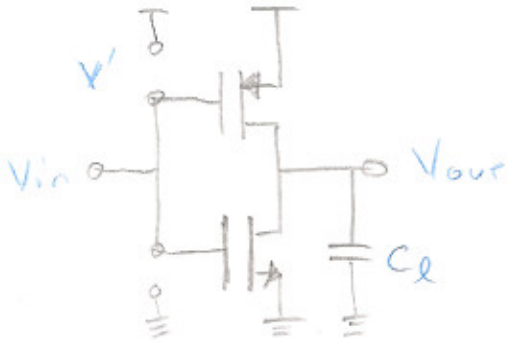


to discharge the cap. faster, we need to increase Id. However this increases Power and heat of the structure.

ENHANCEMENT LOAD



if $V_{in} = V_{in}^{\circ}$
$V' > V_T$
if $V_{in} = V_{in}'$
$V' < V_T$



$$dV_c = \frac{1}{C} i_c(t)\, dt$$

$$\int_{V_{out}^{\circ}}^{V_{out}'} dV_c = \frac{1}{C} \int_{0}^{\Delta t_{0\to 1}} I_{dp}\, dt$$

$$I_{dp} = f(V_{GSP})$$

$$V_{out}' - V_{out}^{\circ} = \frac{I_{dp}}{C} \cdot \Delta t_{0\to 1}$$

$$\Delta t_{0\to 1} = C_l \frac{V_{out}' - V_{out}^0}{I_{dp}}$$

$V_{in} = V_{in}' \approx V_{dd}$

$V' \approx 0$

n-MOS is Active

p-MOS is cutt off.

$$\int_{V_{out}'}^{V_{out}^0} dV_c = \frac{-1}{C_l} \int_0^{\Delta t_{1\to 0}} I_{dn}\, dt$$

$I_{dn} = f(V_{GSn})$

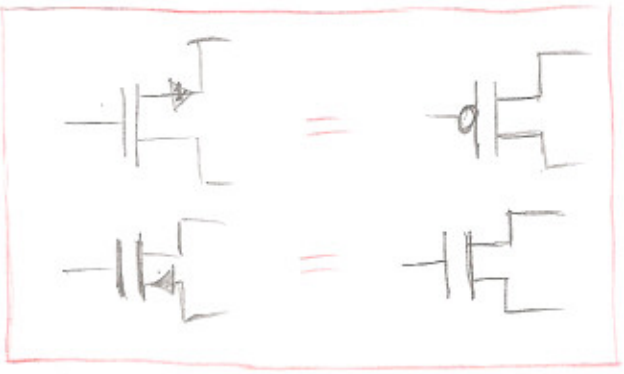
$V_{GS,N} = V_{dd}$

note minus since

$$V_{out}^0 - V_{out}' = \frac{-1}{C_l} I_{dn} \cdot (-\Delta t_{1\to 0})$$

$$\Delta t_{0\to 1} = \frac{V_{out}' - V_{out}^0}{I_{dn}} C_l$$

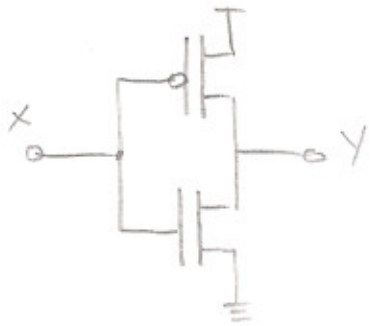
note



however use only ones with arrows for exam so we show drain and source.

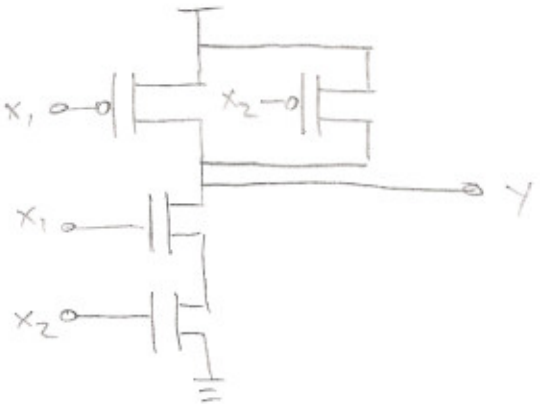
CMOS

NOT



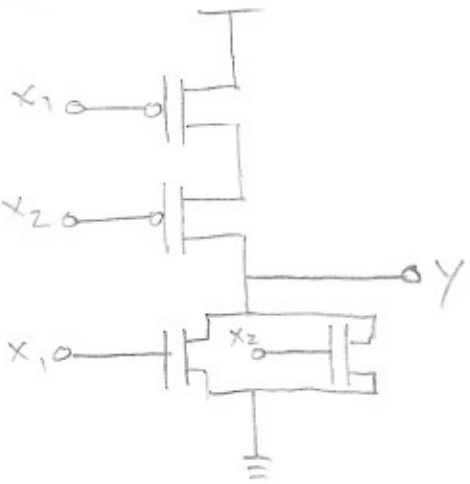
$$X = \overline{Y}$$

NAND



$$\overline{X_1 \cdot X_2} = Y.$$

NOR



$$\overline{X_1 + X_2} = Y$$